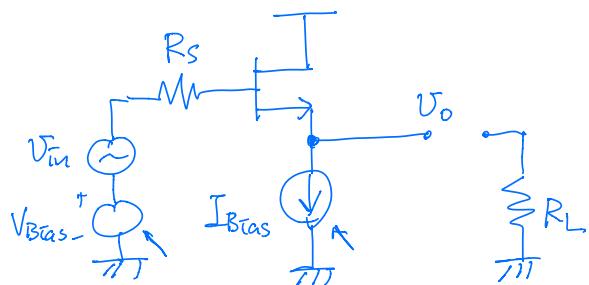


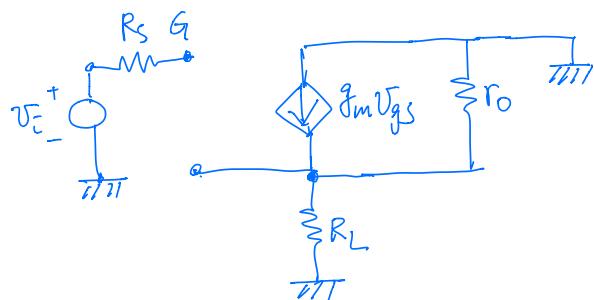
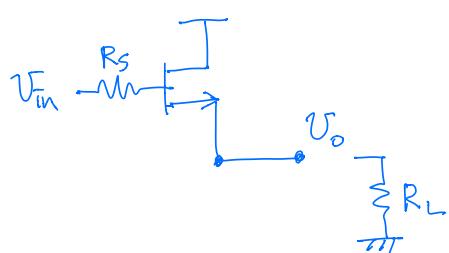
Common Source (CS)

Common Gate (CG)

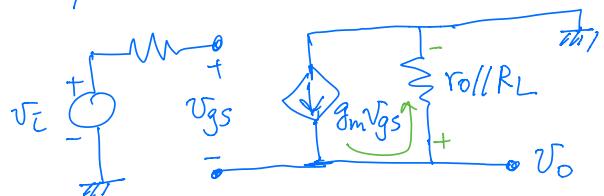
Common Drain (CD)



AC



Simplify



$$V_{gs} = V_i$$

$$V_o = g_m V_{gs} (r_o // R_L) = g_m (V_i - V_o) (r_o // R_L)$$

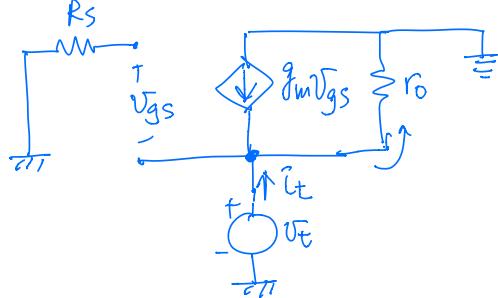
$$g_m r_o \gg 1$$

$$\frac{V_o}{V_i} = \frac{g_m (r_o // R_L)}{1 + g_m (r_o // R_L)} \approx 1$$

$$g_m (r_o // R_L) \gg 1$$

$$R_{in} = \infty$$

$$R_{out}$$



$$V_{gs} = 0 - V_t = -V_t$$

$$\text{KCL at source} \quad i_t + g_m V_{gs} = \frac{V_t}{R_o}$$

$$i_t - g_m V_t = \frac{V_t}{R_o}$$

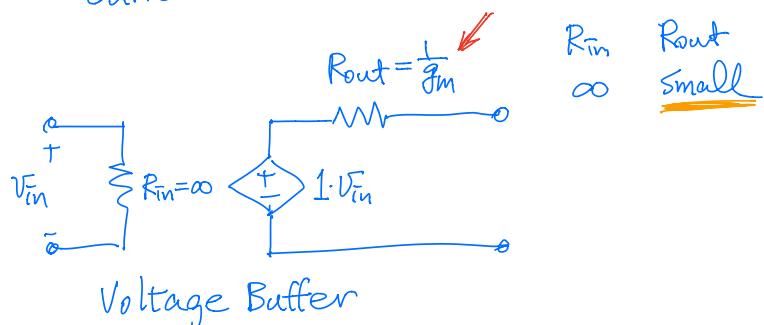
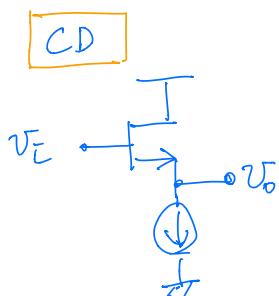
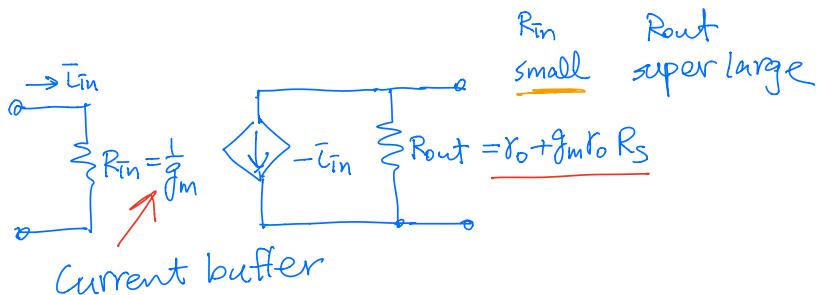
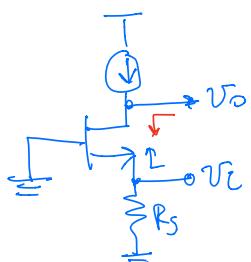
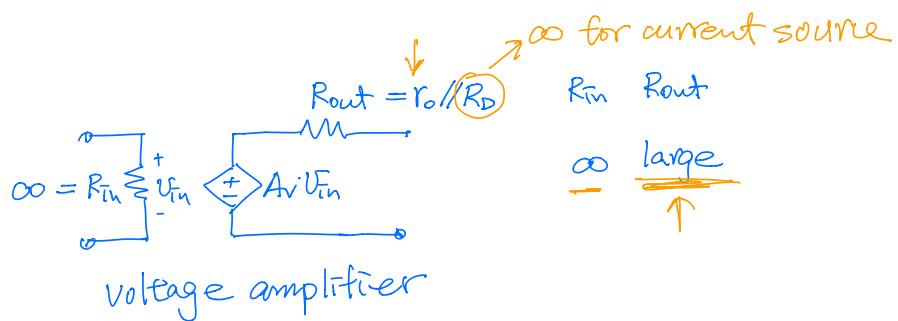
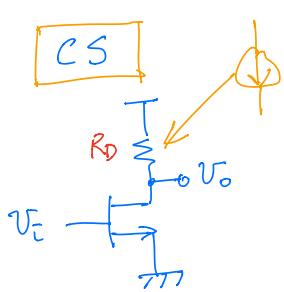
$$R_{out} = \frac{V_t}{i_t} = \frac{1}{\frac{1}{R_o} + g_m} \approx \frac{1}{g_m}$$

Previously

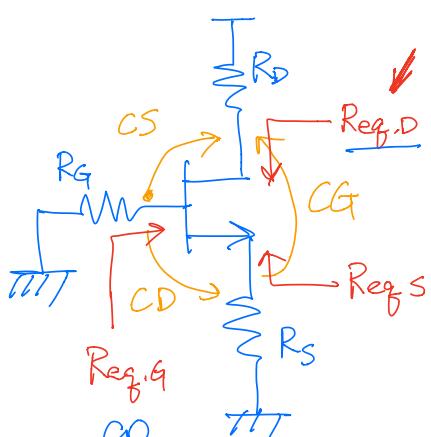
$$r_o \sim 100 \text{ k}\Omega \text{ large}$$

$$g_m \sim \text{mS}$$

$$\frac{1}{g_m} \sim \text{k}\Omega \text{ small}$$



Consider Generally loaded FET

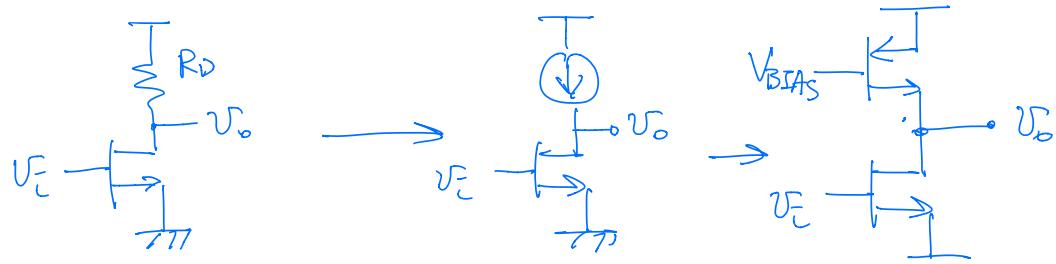


$$R_{eq} = r_o + g_m r_o R_s$$

large

$R_{eq} = \frac{1}{g_m}$

## Current Mirrors



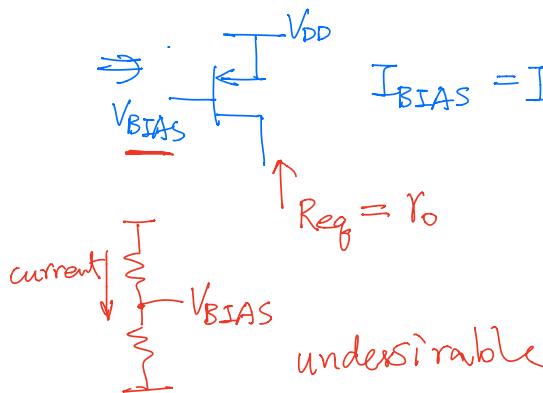
$$A_v: -g_m(r_{\text{in}} \parallel R_D)$$

$$\approx -g_m R_D$$

$$R_{\text{out}}: r_{\text{in}} \parallel R_D \approx R_D$$

$$r_o \uparrow$$

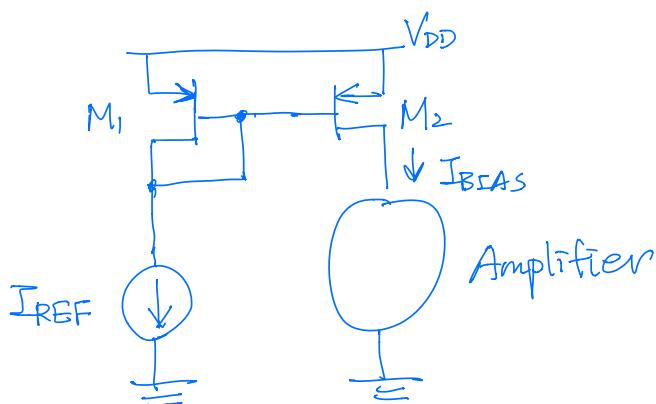
What is ?



$$I_{\text{BIAS}} = I_{D,\text{PMOS}} = \frac{1}{2} k_p [(V_{DD} - V_{\text{BIAS}}) - |V_{t,p}|]^2$$

- ① Power consumption
- ② IC. Resistor  $\rightarrow$  transistor

## Current Mirror



M<sub>1</sub>: "Diode connection"

G — D

$\Rightarrow M_1$  always in Sat.

$$V_{G_1} = V_D$$

$$I_{\text{REF}} = \frac{k_p}{2} [(V_{DD} - V_{G_1}) - |V_{t,p}|]^2$$

M<sub>2</sub>: Biased with  $V_{G_2} = V_{G_1}$

If  $M_1$  and  $M_2$  are same transistors ,

$$I_{BIAS} = I_{REF}$$

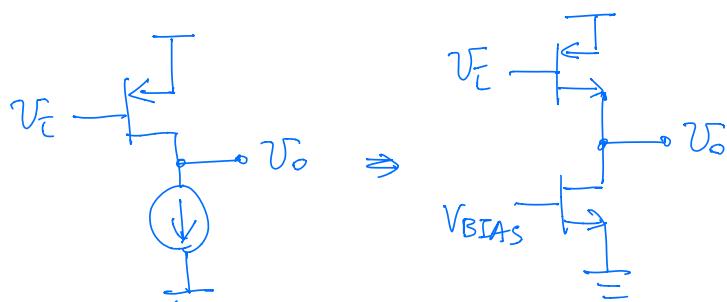
How do we obtain different current ?

$$I_D = \frac{1}{2} k'_p \left( \frac{W}{L} \right) (V_{DD})^2$$

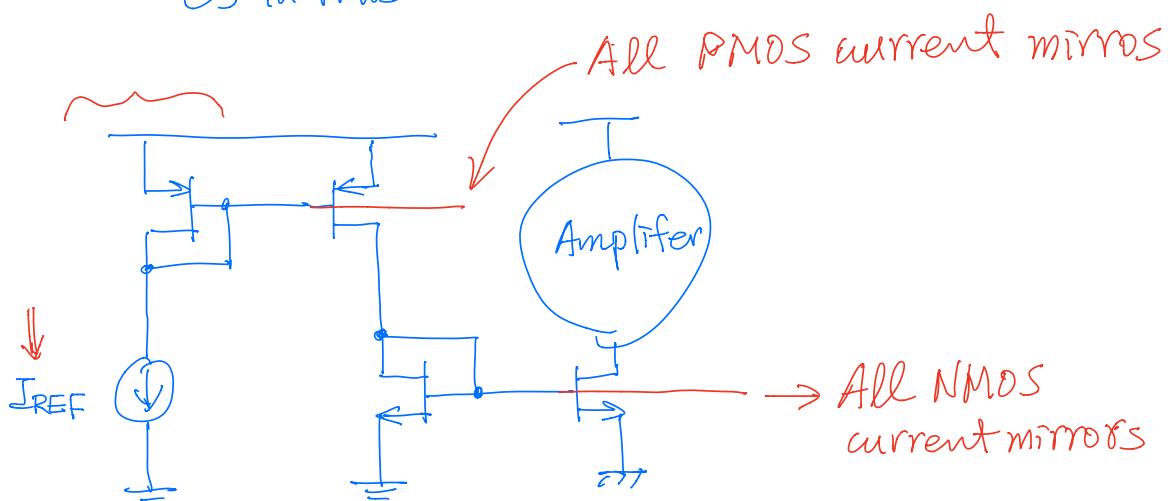
$\uparrow$                      $\curvearrowright$   
 $k_p' C_{ox}$       Vary  $\left( \frac{W}{L} \right)$  of  $M_2$   
 $\uparrow$

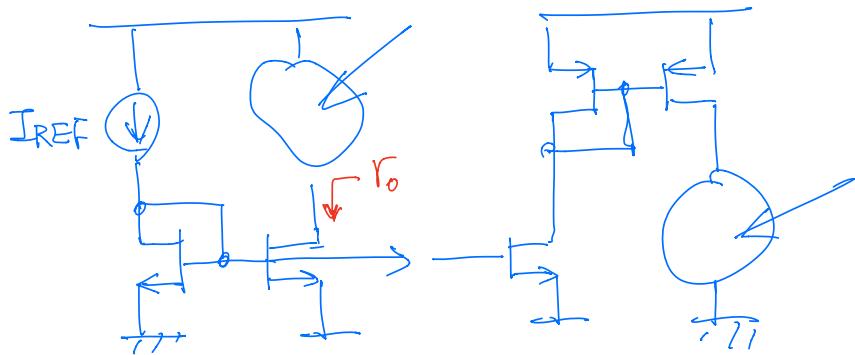
$$I_{BIAS} = I_{REF} \frac{\left( \frac{W}{L} \right)_2}{\left( \frac{W}{L} \right)_1}$$

Need 

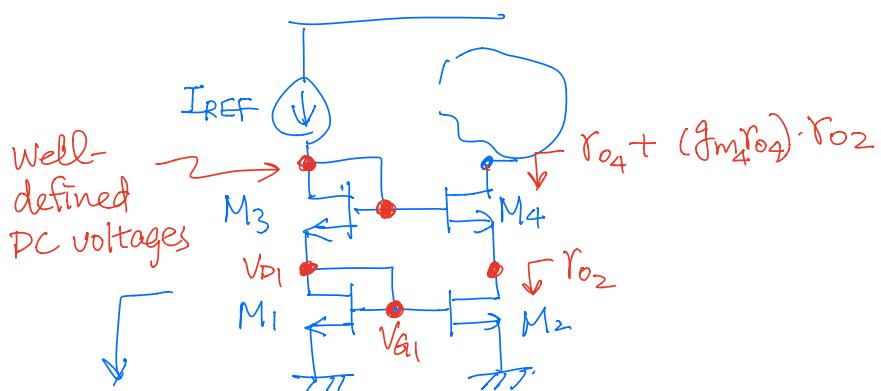
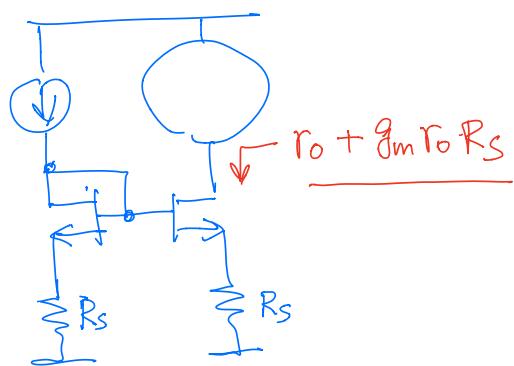


CS in PMOS





Super large Equivalent resistance



Disadvantage: Output swing smaller  
Both M\_2 and M\_4 need to be  
kept at Saturation

What is  $V_{\text{out}}$  minimum?  $V_{\text{out}, \min} = V_{G4} - V_{t,n} = V_{o,4}$

$$V_{G1} = V_{D1}$$

$$V_{G3} = V_{D3}$$

$$I_{\text{REF}} = \frac{1}{2} k_n V_{o,V_i}^2 \Rightarrow \text{know } V_{o,1} = V_{GS1} - V_{tn} \Rightarrow V_{G1}$$
$$V_{o,3} = V_{GS3} - V_{tn} \Rightarrow V_{GS3}$$

$$V_{G3} = V_{S3} + V_{o,V_3} + V_{tn}$$
$$= V_{E_{o,V_1}} + V_{o,V_3} + V_{tn}$$
$$= V_{o,1} + V_{tn} + V_{o,V_3} + V_{tn}$$